WHAT IS CLAIMED IS:

1. A boosting circuit having charge pump circuits for generating a boosting voltage with respect to a predetermined potential by allowing charge to move through a charge transfer transistor in synchronization with a clock signal input through a capacitor, comprising:

a first charge pump circuit group in which the charge pump circuits are connected in series of n stages (n is an integer of 2 or more) to each other;

a second charge pump circuit group in which the charge pump circuits are connected in series of m stages (m is an integer of 2 or more) to each other; and

a stage-number switching circuit for switching an output terminal of the first charge pump circuit group and an input terminal of the second charge pump circuit group between a connected state and an unconnected state in accordance with a stage-number switching control signal, in such a manner that the first charge pump circuit group and the second charge pump circuit group are connected in series with each other and the second charge pump circuit group outputs a first boosting voltage, or the first charge pump circuit group and the second charge pump circuit group are connected in parallel with each other and the first and second charge pump circuit groups output a second boosting voltage,

wherein the stage-number switching circuit includes:

a switching transistor having a current channel connected between the output terminal of the first charge pump circuit group and the input terminal of the second charge pump circuit group; and

a capacitor, one electrode of which is supplied with a clock signal synchronized with a clock signal input to the charge pump circuit and the other electrode of which is connected to a gate of the switching transistor, and

in a case where the stage-number switching control signal is at a first voltage level, the switching transistor is turned on with a supplied clock signal, and in a case where the stage-number switching control signal is at a second voltage level, the switching transistor is turned off.

2. The boosting circuit according to claim 1, wherein in a case where the stage-number switching control signal is at the first voltage level, the stage-number switching circuit is allowed to be operated in the same way as

in one stage of charge pump circuit by synchronizing the stage-number switching circuit with a clock signal to be input.

3. The boosting circuit according to claim 1, wherein the stage-number switching circuit comprises:

a level shift circuit that is supplied with the first or second boosting voltage as a supply voltage to shift a voltage level of the stage-number switching control signal; and

a switch circuit for setting a potential of the input terminal of the second charge pump circuit group to be the same as a potential of the input terminal of the first charge pump circuit group with a signal output from the level shift circuit, in a case where the stage-number switching control signal is at the second voltage level.

4. The boosting circuit according to claim 1, wherein the stage-number switching circuit comprises a gate circuit for enabling or disabling a clock signal to be supplied, in accordance with the stage-number switching control signal.

5. The boosting circuit according to claim 1, further comprising:

a first reverse flow preventing transistor connected between the output terminal of the first charge pump circuit group and an output terminal of the boosting circuit; and

a second reverse flow preventing transistor connected between an output terminal of the second charge pump circuit group and an output terminal of the boosting circuit.

6. The boosting circuit according to claim 5, further comprising a smoothing capacitor connected to the output terminal of the boosting circuit.

7. The boosting circuit according to claim 1, wherein the first and second charge pump circuit groups are composed of 2-stage charge pump circuits connected in series, and clock signals supplied to the 2-stage charge pump circuits are composed of 4 kinds of clock signals having different phases.

8. The boosting circuit according to claim 1, wherein the charge-pump circuit comprises:

a charge transfer transistor having a current channel connected between an input terminal and an output terminal of the charge pump circuit;

a threshold canceling transistor having a current channel connected to the input terminal and a gate of the charge transfer transistor;

a first coupling capacitor, one electrode of which is connected to a gate of the charge transfer transistor and the other electrode of which is supplied with a clock signal; and

a second coupling capacitor, one electrode of which is connected to a gate of the threshold canceling transistor and the other electrode of which is supplied with a clock signal.

9. The boosting circuit according to claim 1, wherein a transistor constituting the charge pump circuit is an N-channel MOS transistor, and the boosting circuit outputs a boosted positive voltage.

10. The boosting circuit according to claim 1, wherein a transistor constituting the charge pump circuit is a P-channel MOS transistor, and the boosting circuit outputs a boosted negative voltage.

11. The boosting circuit according to claim 9, wherein a transistor constituting the stage-number switching circuit is an N-channel MOS transistor.

12. The boosting circuit according to claim 10, wherein a transistor constituting the stage-number switching circuit is a P-channel MOS transistor.

13. A boosting circuit having charge pump circuits for generating a boosting voltage with respect to a predetermined potential by allowing charge to move through a charge transfer transistor in synchronization with a clock signal input through a capacitor, comprising:

a first charge pump circuit group in which the charge pump circuits are connected in series of n stages (n is an integer of 2 or more) to each other;

a second charge pump circuit group in which the charge pump circuits are connected in series of m stages (m is an integer of 2 or more) to each other;

a third charge pump circuit group connected in series with the second charge pump circuit group, in which the charge pump circuits are connected in series of p stages (p is an integer of 2 or more) to each other, and which outputs a first or second boosting voltage;

a first stage-number switching circuit for switching an output terminal of the first charge pump circuit group and an input terminal of the second charge pump circuit group between a connected state and an unconnected state in accordance with a first stage-number switching control signal;

a gate circuit for enabling or disabling a clock signal supplied to the second charge pump circuit group in accordance with the first stage-number switching control signal; and

a second stage-number switching circuit for switching the output terminal of the first charge pump circuit group and an input terminal of the third charge pump circuit group between a connected state and an unconnected state, in accordance with a second stage-number switching control signal that is a logic inverse signal of the first stage-number switching control signal,

wherein the first stage-number switching circuit includes:

a first switching transistor having a current channel connected between the output terminal of the first charge pump circuit group and the input terminal of the second charge pump circuit group; and

a first capacitor, one electrode of which is supplied with a clock signal synchronized with a clock signal input to the charge pump circuit, and the other electrode of which is connected to a gate of the first switching transistor,

in a case where the first stage-number switching control signal is at a first voltage level, the first switching transistor is turned on with a supplied clock signal, and in a case where the first stage-number switching control signal is at a second voltage level, the first switching transistor is turned off,

wherein the second stage-number switching circuit includes:

a second switching transistor having a current channel connected between the output terminal of the first charge pump circuit group and the input terminal of the third charge pump circuit group; and

a second capacitor, one electrode of which is supplied with a clock signal synchronized with a clock signal input to the charge pump circuit, and the other electrode of which is connected to a gate of the second switching

transistor,

in a case where the second stage-number switching control signal is at the first voltage level, the second switching transistor is turned on with a supplied clock signal, and in a case where the second stage-number switching control signal is at the second voltage level, the second switching transistor is turned off.

14. The boosting circuit according to claim 13, wherein in a case where the stage-number switching control signal is at the first voltage level, the stage-number switching circuit is allowed to be operated in the same way as in one stage of charge pump circuit by synchronizing the stage-number switching circuit with a clock signal to be input.

15. The boosting circuit according to claim 13, wherein the stage-number switching circuit includes a gate circuit for enabling or disabling a clock signal to be supplied, in accordance with the stage-number switching control signal.

16. The boosting circuit according to claim 13, further comprising a reverse flow preventing transistor connected between an output terminal of the third charge pump circuit group and an output terminal of the boosting circuit.

17. The boosting circuit according to claim 16, further comprising a smoothing capacitor connected to the output terminal of the boosting circuit.

18. The boosting circuit according to claim 13, wherein the first, second, and third charge pump circuit groups are composed of 2-stage charge pump circuits connected in series, and clock signals supplied to the 2-stage charge pump circuits are composed of 4 kinds of clock signals having different phases.

19. The boosting circuit according to claim 13, wherein the charge-pump circuit comprises:

a charge transfer transistor having a current channel connected between an input terminal and an output terminal of the charge pump circuit;

a threshold canceling transistor having a current channel connected

to the input terminal and a gate of the charge transfer transistor;

a first coupling capacitor, one electrode of which is connected to a gate of the charge transfer transistor and the other electrode of which is supplied with a clock signal; and

a second coupling capacitor, one electrode of which is connected to a gate of the threshold canceling transistor and the other electrode of which is supplied with a clock signal.

20. The boosting circuit according to claim 13, wherein a transistor constituting the charge pump circuit is an N-channel MOS transistor, and the boosting circuit outputs a boosted positive voltage.

21. The boosting circuit according to claim 13, wherein a transistor constituting the charge pump circuit is a P-channel MOS transistor, and the boosting circuit outputs a boosted negative voltage.

22. The boosting circuit according to claim 20, wherein a transistor constituting the stage-number switching circuit is an N-channel MOS transistor.

23. The boosting circuit according to claim 21, wherein a transistor constituting the stage-number switching circuit is a P-channel MOS transistor.

24. A boosting circuit having charge pump circuits for generating a boosting voltage with respect to a predetermined potential by allowing charge to move through a charge transfer transistor in synchronization with a clock signal input through a capacitor, comprising:

a first charge pump circuit group in which the charge pump circuits are connected in series of n stages (n is an integer of 2 or more) to each other;

a second charge pump circuit group in which the charge pump circuits are connected in series of m stages (m is an integer of 2 or more) to each other; and

a stage-number switching circuit for switching an output terminal of the first charge pump circuit group and an input terminal of the second charge pump circuit group between a connected state and an unconnected state in accordance with a stage-number switching control signal, in such a

manner that the first charge pump circuit group and the second charge pump circuit group are connected in series with each other and the second charge pump circuit group outputs a first boosting voltage, or the first charge pump circuit group and the second charge pump circuit group are connected in parallel with each other and the first and second charge pump circuit groups output a second boosting voltage,

wherein the stage-number switching circuit includes:

a level shift circuit that is supplied with the first or second boosting voltage as a supply voltage to shift a voltage level of the stage-number switching control signal; and

a switch circuit for switching an output terminal of the first charge pump circuit group and an input terminal of the second charge pump circuit group between a connected state and an unconnected state, in accordance with a signal output from the level shift circuit.

25. The boosting circuit according to claim 24, wherein the switch circuit sets a potential of the input terminal of the second charge pump circuit group to be the same as a potential of the input terminal of the first charge pump circuit group with a signal output from the level shift circuit, in a case where the stage-number switching control signal is at the second voltage level.

26. The boosting circuit according to claim 24, further comprising:

a first reverse flow preventing transistor connected between the output terminal of the first charge pump circuit group and an output terminal of the boosting circuit; and

a second reverse flow preventing transistor connected between an output terminal of the second charge pump circuit group and an output terminal of the boosting circuit.

27. The boosting circuit according to claim 26, further comprising a smoothing capacitor connected to the output terminal of the boosting circuit.

28. The boosting circuit according to claim 24, wherein the first and second charge pump circuit groups are composed of 2-stage charge pump circuits connected in series, and clock signals supplied to the 2-stage charge pump circuits are composed of 4 kinds of clock signals having different phases.

29. The boosting circuit according to claim 24, wherein the charge-pump circuit comprises:

a charge transfer transistor having a current channel connected between an input terminal and an output terminal of the charge pump circuit;

a threshold canceling transistor having a current channel connected to the input terminal and a gate of the charge transfer transistor;

a first coupling capacitor, one electrode of which is connected to a gate of the charge transfer transistor and the other electrode of which is supplied with a clock signal; and

a second coupling capacitor, one electrode of which is connected to a gate of the threshold canceling transistor and the other electrode of which is supplied with a clock signal.

30. The boosting circuit according to claim 24, wherein a transistor constituting the charge pump circuit is an N-channel MOS transistor, and the boosting circuit outputs a boosted positive voltage.

31. The boosting circuit according to claim 24, wherein a transistor constituting the charge pump circuit is a P-channel MOS transistor, and the boosting circuit outputs a boosted negative voltage.

32. The boosting circuit according to claim 30, wherein a transistor constituting the stage-number switching circuit is an N-channel MOS transistor.

33. The boosting circuit according to claim 31, wherein a transistor constituting the stage-number switching circuit is a P-channel MOS transistor.

34. A non-volatile semiconductor storage device, comprising:

a boosting circuit;

a non-volatile memory cell array that is supplied with a boosting voltage from the boosting circuit; and

a stage-number switching control circuit for switching a voltage level of a stage-number switching control signal to a first or second voltage level, in accordance with an operation mode of a memory,

wherein the boosting circuit has charge pump circuits for generating a boosting voltage with respect to a predetermined potential by allowing charge to move through a charge transfer transistor in synchronization with a clock signal input through a capacitor, the boosting circuit comprising:

a first charge pump circuit group in which the charge pump circuits are connected in series of n stages (n is an integer of 2 or more) to each other;

a second charge pump circuit group in which the charge pump circuits are connected in series of m stages (m is an integer of 2 or more) to each other; and

a stage-number switching circuit for switching an output terminal of the first charge pump circuit group and an input terminal of the second charge pump circuit group between a connected state and an unconnected state in accordance with a stage-number switching control signal, in such a manner that the first charge pump circuit group and the second charge pump circuit group are connected in series with each other and the second charge pump circuit group outputs a first boosting voltage, or the first charge pump circuit group and the second charge pump circuit group are connected in parallel with each other and the first and second charge pump circuit groups output a second boosting voltage,

wherein the stage-number switching circuit includes:

a switching transistor having a current channel connected between the output terminal of the first charge pump circuit group and the input terminal of the second charge pump circuit group; and

a capacitor, one electrode of which is supplied with a clock signal synchronized with a clock signal input to the charge pump circuit and the other electrode of which is connected to a gate of the switching transistor, and

in a case where the stage-number switching control signal is at a first voltage level, the switching transistor is turned on with a supplied clock signal, and in a case where the stage-number switching control signal is at a second voltage level, the switching transistor is turned off.

35. A non-volatile semiconductor storage device, comprising:

a boosting circuit;

a non-volatile memory cell array that is supplied with a boosting voltage from the boosting circuit; and

a stage-number switching control circuit for switching a voltage level of a stage-number switching control signal to a first or second voltage level, in accordance with an operation mode of a memory,

wherein the boosting circuit has charge pump circuits for generating a boosting voltage with respect to a predetermined potential by allowing charge to move through a charge transfer transistor in synchronization with a clock signal input through a capacitor, the boosting circuit comprising:

a first charge pump circuit group in which the charge pump circuits are connected in series of n stages (n is an integer of 2 or more) to each other;

a second charge pump circuit group in which the charge pump circuits are connected in series of m stages (m is an integer of 2 or more) to each other;

a third charge pump circuit group connected in series with the second charge pump circuit group, in which the charge pump circuits are connected in series of p stages (p is an integer of 2 or more) to each other, and which outputs a first or second boosting voltage;

a first stage-number switching circuit for switching an output terminal of the first charge pump circuit group and an input terminal of the second charge pump circuit group between a connected state and an unconnected state in accordance with a first stage-number switching control signal;

a gate circuit for enabling or disabling a clock signal supplied to the second charge pump circuit group in accordance with the first stage-number switching control signal; and

a second stage-number switching circuit for switching the output terminal of the first charge pump circuit group and an input terminal of the third charge pump circuit group between a connected state and an unconnected state, in accordance with a second stage-number switching control signal that is a logic inverse signal of the first stage-number switching control signal,

wherein the first stage-number switching circuit includes:

a first switching transistor having a current channel connected between the output terminal of the first charge pump circuit group and the input terminal of the second charge pump circuit group; and

a first capacitor, one electrode of which is supplied with a clock signal synchronized with a clock signal input to the charge pump circuit,

and the other electrode of which is connected to a gate of the first switching transistor,

in a case where the first stage-number switching control signal is at a first voltage level, the first switching transistor is turned on with a supplied clock signal, and in a case where the first stage-number switching control signal is at a second voltage level, the first switching transistor is turned off,

wherein the second stage-number switching circuit includes:

a second switching transistor having a current channel connected between the output terminal of the first charge pump circuit group and the input terminal of the third charge pump circuit group; and

a second capacitor, one electrode of which is supplied with a clock signal synchronized with a clock signal input to the charge pump circuit, and the other electrode of which is connected to a gate of the second switching transistor,

in a case where the second stage-number switching control signal is at the first voltage level, the second switching transistor is turned on with a supplied clock signal, and in a case where the second stage-number switching control signal is at the second voltage level, the second switching transistor is turned off.

36. A non-volatile semiconductor storage device, comprising:

a boosting circuit;

a non-volatile memory cell array that is supplied with a boosting voltage from the boosting circuit; and

a stage-number switching control circuit for switching a voltage level of a stage-number switching control signal to a first or second voltage level, in accordance with an operation mode of a memory,

wherein the boosting circuit has charge pump circuits for generating a boosting voltage with respect to a predetermined potential by allowing charge to move through a charge transfer transistor in synchronization with a clock signal input through a capacitor, the boosting circuit comprising:

a first charge pump circuit group in which the charge pump circuits are connected in series of n stages (n is an integer of 2 or more) to each other;

a second charge pump circuit group in which the charge pump circuits are connected in series of m stages (m is an integer of 2 or more) to each other; and

a stage-number switching circuit for switching an output terminal of the first charge pump circuit group and an input terminal of the second charge pump circuit group between a connected state and an unconnected state in accordance with a stage-number switching control signal, in such a manner that the first charge pump circuit group and the second charge pump circuit group are connected in series with each other and the second charge pump circuit group outputs a first boosting voltage, or the first charge pump circuit group and the second charge pump circuit group are connected in parallel with each other and the first and second charge pump circuit groups output a second boosting voltage,

wherein the stage-number switching circuit includes:

a level shift circuit that is supplied with the first or second boosting voltage as a supply voltage to shift a voltage level of the stage-number switching control signal; and

a switch circuit for switching an output terminal of the first charge pump circuit group and an input terminal of the second charge pump circuit group between a connected state and an unconnected state, in accordance with a signal output from the level shift circuit.